Remarks:

Reconsideration of the claims as amended are respectfully requested. Claims 1-15 are pending in the application. Claims 1-4 stand rejected. Claims 1-4 have been cancelled, and Claims 5-11 have been amended. New claims 4-15 have been added. Support is found in the application as filed, and no new matter has been added.

In order to advance prosecution of the present application, Applicant has cancelled the rejected claims 1-4. Also, in response to the examiners objections, applicant has amended Claims 5-11. This is intended as a significant attempt to move the prosecution of this application forward to allowance. The Abstract has also been amended to include the limitations of amended Claim 5.

The office action objects to Claims 5-15, stating that "[i]t is not seen where in the drawings "the third segmented series of resistors" includes a current source." In support, as stated in the application, on Page 2, lines 17-30, the detailed description describes the invention in terms of "dual current devices initially load, then subsequently unload a cascade of resistor elements connected to the secondary or successive segmented elements..." to provide reduced errors in the primary or preceding elements:

> The invention is directed to an improved segmented digital to analog converter configured with a novel method of compensating current flow in secondary or successive segmented elements. In operation, dual current devices initially load, then subsequently unload a cascade of resistor networks connected to the secondary or successive voltage segmenting elements, preventing the perturbation of precise operation of the primary or preceding elements. The improved converter removes substantially all errors from the secondary or successive cascade of connected resistor networks, and does not substantially disturb the circuit as a whole. In contrast to conventional approaches, the improved converter obviates the need for a buffer or amplifier to isolate the secondary and successive voltage segmenting elements from the primary or preceding elements. Clearing out errors existing in the secondary or successive elements serves to prevent errors that would previously cause errors in the primary or preceding elements, obviating the need for isolation of the secondary or successive elements.

This language was intended to describe two or more segmented sets of resistors connected at either ends by parallel current devices as now claimed in the amended claims. Given the prior art, the claims have been limited to more than two segmented sets of resistors, in fact three or

more segmented sets of resistor banks, each connected at opposite ends by parallel current devices. Furthermore, the application on Page 4, lines 24-27 states:

> Referring to Figure 2, one means is illustrated by which that current may be made, namely by biasing the first resistor network between low impedance points of a current source and deriving a scaled version of that current from a parallel connection of PMOS and NMOS devices.

Picking up on that concept, the application on Page 5, beginning at line 22, the second and third additional segmented sets of resistors are included in the circuit to substantially reduce systematic error resulting from operation:

> However, in the improved circuit illustrated in Figure 2, and according to the invention, the devices 214 and 216 each form part of a cascoded current source providing this current. Hence no current needs to flow out of the first set of resistors. Hence there is no disturbance. This is the principle and may be repeated again for a third set of resistors and can be repeated for successive sets of resistors (not shown). In this circuit there is substantially no systematic error resulting from operation. Given that the currents are accurate, the error is substantially zero and independent of the resistance of the switches in the "on" or closed position used to connect the second set of segmented elements to the first set of segmented elements. This is also true for a second set connected to the third set, and other successive sets that may be connection in other circuits.

This further specifies the third set of segmented resistors, as well as additional sets. Devices 214 and 216 described here are understood as the parallel PMOS and NMOS devices described on page 4, cited above. Similar parallel PMOS/NMOS devices also exist at either end of each segmented set of resistors, including set 218. As illustrated and claimed, each segmented set of resistors is connected at opposite ends with a current source. The third set of segmented resistors is illustrated in Figure 2 as item 218, the third set of segmented resistors. The two current sources one connected immediately above the third set of segmented resistors 218 and the other current source below the third set of segmented resistors. These are the same type of current sources as devices 214 and 216 described above. Claims 5-15 now further clarify this concept, and also expands to further cover segments as disclosed in the application as filed. Again, no new matter has been added. The examiner stated that claims 4-15 (Applicant believes that the Examine meant to state 5-15) would be allowable if the objection were overcome. Applicant submits that this objection has been overcome and respectfully requests the withdrawal of the objection.

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Applicants respectfully submit that all of the claims as amended are in condition for allowance and, accordingly, requests the allowance of amended claims 5-15. If the Examiner finds that a telephone conference would expedite the prosecution of this application, the Examiner is invited to telephone Dave Stevens for a telephone conference at the number provided below.

The Commissioner is hereby authorized to charge any additional fees due or credit any overpayment to Deposit Account No. 50-2421.

Sincerely,

Dated May 9, 2005

David R. Stevens
Reg. No. 38,626

Stevens Law Group
P.O. Box 1667
San Jose, CA 95109
Tel (408) 288-7588
Fax (408) 288-7542